

## **Abstract**

A method and system for storing and modifying register transfer language (RTL) described logic types. Upon a declaration of a signal interconnect, a language extension of a register transfer language is defined for the signal interconnect based on the signal `[[interconnect"s]] interconnect's` type. The language extensions allow different signal interconnect types, such as those used with field programmable gate arrays (FPGA) and standard cells, to be stored in a same file array hierarchy. This storage facilitates changing logic types, thus ultimately resulting in an integrated circuit (IC) that is either smaller (using more standard cells) or more flexible (using more FPGA cells). The transition from one RTL type to another is performed within the physical design cycle, in which wiring, timing and placement of components (information) is performed before masking out the final chip design.